WHAT IS CLAIMED IS:

1. A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising the steps of:

forming a gate wire on an insulating substrate by a first photolithography process;

forming a quadruple layer including a gate insulating layer, a semiconductor layer, an ohmic contact layer and a data conductor layer on the substrate and the gate wire by a second photolithography process;

forming a conductive pattern on the data conductor layer by a third photolithography process;

etching the portion of the data conductor layer not covered by the conductive pattern to form a data wire;

etching the ohmic contact layer not covered by the data wire; and

forming a passivation layer pattern on the conductive pattern by a fourth photolithography process.

2. The method of claim 1, wherein:

the gate wire includes a plurality of gate lines extending to a first direction, gate electrodes that are branches of the gate lines and gate pads connected to an end of each of the gate lines and receiving scanning signals from an external circuit;

the quadruple layer has first contact holes exposing the gate pads; and

the passivation layer has second contact holes exposing the first contact holes.

3. The method of claim 1, wherein:

the gate wire includes a plurality of gate lines extending to a first direction, gate electrodes that are branches of the gate lines and gate pads connected to an end of each of the gate lines and receiving scanning signals from an external circuit;

the quadruple layer has first contact holes exposing the gate pads;

the conductive pattern includes first conductive patterns connected to the gate pads through the first contact holes; and

the passivation layer has second contact holes exposing the first conductive patterns.

4. The method of claim 1, wherein:

the gate wire includes a plurality of gate lines extending to a first direction, gate electrodes that are branches of the gate lines and gate pads connected to an end of each of the gate lines and receiving scanning signals from an external circuit;

the data wire includes a plurality of data lines extending to a second direction to cross the gate lines, data pads connected to an end of each of the data lines and receiving image signals from an external circuit, source electrodes connected to the data lines and located adjacent to the gate electrodes, and drain electrodes located at the opposite side of the source electrodes with respect to the gate electrodes;

the conductive pattern includes a plurality of first conductive patterns formed on the data lines, the source electrodes and the data pads, second conductive patterns formed on the drain electrodes, and pixel electrodes connected to the second conductive patterns and formed in the area

surrounded by the gate lines and the data lines; and

the passivation layer has first openings exposing the pixel electrodes and second openings exposing the first conductive patterns on the data pads.

5. The method of claim 4, wherein the passivation layer has third openings exposing parts of the semiconductor layer between the adjacent two data lines, and further comprising a step of etching the exposed portions of the semiconductor layer to separate the semiconductor layer under the two data lines.

6. The method of claim 5, wherein the pixel electrode is overlapped with the previous gate line and the portion of the semiconductor layer interposed between the pixel electrode and the gate line is isolated from the other portion of the semiconductor layer.

7. The method of claim 5, wherein the gate insulating layer includes first portions formed between the gate pads and between the data pads, the passivation layer has fourth openings exposing the first portions of the gate insulating layer, and the portions of the semiconductor layer located on the first portions of the gate insulating layer is removed to separate the portions of the semiconductor layer between the gate pads and between the data pads.

8. The method of claim 5, wherein the passivation layer covers the edge of the pixel electrode.

9. The method of claim 5, wherein the first opening exposes the edge of the pixel electrode.

10. The method of claim 5, wherein a storage wire overlapping the pixel electrodes is formed on the substrate, the quadruple layer is formed on the

storage wire, and the portions of the semiconductor layer interposed between the storage wire and the pixel electrodes are isolated from the other portions of the semiconductor layer.

11. The method of claim 5, wherein the passivation layer has a plurality of trenchs exposing the portions of the semiconductor layer between the first conductive patterns and the pixel electrodes and between the adjacent pixel electrodes, and further comprising a step of etching the exposed semiconductor layer through the trench.

12. The method of claim 11, wherein the gate line comprises two main lines and branches connecting the two main lines, and the pixel electrode overlaps a part of the gate line.

13. The method of claim 11, wherein the source electrode has a concave part, and an end of the drain electrode is located in the concave part.

14. The method of claim 1, wherein the conductive pattern is made of a transparent conductor.

15. The method of claim 14, wherein the conductive pattern is made of indium-tin-oxide.

16. The method of claim 1, wherein forming the quadruple layers comprises the substeps of:

coating a photoresist layer on the data conductor layer;

patterning the photoresist layer to have a thickness that varies depending on the location by exposure and development;

etching the quadruple layers along with the photoresist layer pattern to expose the gate pad, to form a data wire of which source electrode and drain

electrode are not separated, and to expose the portion of the gate insulating layer between the data wires.

17. The method of claim 16, wherein the first portion that is the thinnest portion of the photoresist layer is formed on the gate pad, the second portion that is the thickest portion is formed on the data wire of which source electrode and drain electrode are not separated, and the third portion that is thicker than the first portion and thinner than the second portion is formed between the second portions.

18. The method of claim 16, wherein the exposure of the photoresist layer is performed by using a photomask having at least three subparts of which transmittance are different from each other.

19. The method of claim 18, wherein a portion of the gate insulating layer is removed to expose ends of the gate wire by the second photolithography process.

20. The method of claim 19, wherein the conductive pattern includes first conductive patterns contacting the exposed end of the gate wire.

21. The method of claim 20, wherein contact holes exposing the first conductive pattern is formed in the passivation layer by the fourth photolithography process.

22. A thin film transistor array panel for a liquid crystal display comprising:

a gate wire formed on an insulating substrate and including a plurality of gate lines extending to a first direction, gate electrodes connected to the gate line, and gate pads connected to an end of the gate line;

a gate insulating layer having contact holes exposing the gate pad and formed in a matrix shape on the gate wire and the substrate;

a semiconductor layer formed on the gate insulating layer;

a data wire formed on the semiconductor layer and including a plurality of data lines extending to a second direction crossing the gate line, source electrodes adjacent to the gate electrode, drain electrode separated from the data line and the source electrode and located at the opposite side of the source electrode with respect to the gate electrode, and data pads connected to an end of the data line;

a conductive pattern including a plurality of first patterns formed on the source electrode and the data line, second patterns formed on the drain electrode, third patterns formed on the data pad, and pixel electrodes connected to the second pattern; and

a passivation layer formed on the conductive pattern, the semiconductor pattern and the substrate, and having a plurality of first openings exposing the pixel electrode, second openings exposing the gate insulating layer between the two adjacent data lines, third openings located on the gate pad, and fourth openings exposing the third pattern,

wherein the data wire is only formed between the conductive pattern and the semiconductor layer, the semiconductor layer is formed on the whole gate insulating layer except for the portion under the second opening, and the portions of the semiconductor layer under the two adjacent data lines are separated from each other.

23. The thin film transistor array panel of claim 22, further comprising a

contact layer formed between the semiconductor layer and the data wire to have the same layout as the data wire for reducing the contact resistance between the semiconductor layer and the data wire.

24. The thin film transistor array panel of claim 23, wherein the conductive pattern further includes a fourth pattern connected to the gate pad through the contact hole and the third opening.

25. The thin film transistor array panel of claim 23, wherein the pixel electrode is overlapping the adjacent gate line and the portion of the semiconductor layer sandwiched between the pixel electrode and the gate line is isolated from the other portion.

26. The thin film transistor array panel of claim 23, wherein the gate insulating layer includes a first portion formed between the two gate pads and the two data pads, the passivation layer has fifth openings exposing the first portion of the gate insulating layer, and the semiconductor layer is not formed under the fifth opening.

27. The thin film transistor array panel of claim 23, the passivation layer covers the edge of the pixel electrode.

28. The thin film transistor array panel of claim 23, wherein the first opening exposes the edge of the pixel electrode.

29. The thin film transistor array panel of claim 28, further including a storage wire formed on the substrate, overlapped with the pixel electrode and covered by the gate insulating layer, wherein the portion of the semiconductor layer sandwiched between the storage wire and the pixel electrode is isolated from the other portion.

30. The thin film transistor array panel of claim 28, wherein the conductive pattern is made of indium-tin-oxide.

31. A method for manufacturing a thin film transistor array panel, comprising the steps of:

forming a gate wire including a plurality of gate lines and gate pads by a first photolithography process;

depositing a first insulating layer, a semiconductor layer, an ohmic contact layer and a metal layer on the gate wire;

forming a metal layer pattern, an ohmic contact layer pattern, a semiconductor layer pattern and a first insulating layer pattern that have a matrix shape layout overlapping the gate wire except for the gate pad by a second photolithography process;

depositing a transparent conductor layer;

forming a transparent conductor pattern including a pixel electrode, a plurality of redundant date lines, redundant source electrodes, redundant drain electrodes, redundant data pad and redundant gate pad by a third photolithography process;

etching out the portion of the metal layer not covered by the transparent conductor pattern and the ohmic contact layer thereunder;

depositing a second insulating layer;

forming a passivation layer pattern having openings respectively exposing the gate pad, the data pad, the pixel electrode and the portion of the semiconductor layer connecting the adjacent data line; and

etching out the portion of the semiconductor layer exposed through the

openings.

32. The method of claim 31, further including etching the first insulating layer under the exposed portion of the semiconductor layer after the exposed portion of the semiconductor layer is etched out.

33. A method for manufacturing a thin film transistor, comprising the steps of:

forming a gate wire including a plurality of gate lines and gate pads by a first photolithography process;

depositing a first insulating layer, a semiconductor layer, an ohmic contact layer and a metal layer on the gate wire;

patterning the metal layer, the ohmic contact layer, the semiconductor layer and the first insulating layer to form a metal layer pattern, an ohmic contact layer pattern, and a semiconductor layer pattern that are separated into two pieces at least on the gate wire and a first insulating layer pattern covering the gate wire except for the gate pad;

depositing a transparent conductor layer;

forming a transparent conductor layer pattern by a third photolithography process;

etching the portion of the metal layer not covered by the transparent conductor layer pattern and the underlying ohmic contact layer to form a data wire including a plurality of data pads, source and drain electrodes and ohmic contact layer pattern thereunder;

depositing a second insulating layer; and

forming a passivation layer pattern at least having contact holes

exposing the gate pad and the data pad by a fourth photolithography process.

34. The method of claim 33, wherein the second photolithography process comprises the substeps of;

coating a photoresist layer on the metal layer;

forming a photoresist layer pattern having at least three portion of which thickness are different from each other by exposure and development; and

etching the metal layer, the ohmic contact layer, the semiconductor layer and the first insulating layer along with the photoresist layer to remove the first portion that is the thinnest portion of the photoresist layer pattern, and the metal layer, the ohmic contact layer, the semiconductor layer and the first insulating layer thereunder, along with the third portion that is the thicker than the first portion, and the metal layer, the ohmic contact layer and the semiconductor layer thereunder, leaving the layers under the second portion that is the thickest portion intact.

35. The method of claim 34, wherein the exposure of the photoresist layer is performed by using a photomask including at least three subparts of which transmittance are different from each other

36. The method of claim 35, wherein the photomask has slits smaller than the resolution of the stepper.

37. The method of claim 35, wherein the photomask is formed by at least two materials of which transmittance are different from each other.

38. The method of claim 36, wherein the photomask is classified into a first mask to form the gate pad and a second mask to form the elsewhere, and the transmittance of the first mask is different from that of the second mask.

39. The method of claim 37, wherein the photomask is classified into a first mask to form the gate pad and a second mask to form the elsewhere, and the transmittance of the first mask is different from that of the second mask.

40. The method of claim 34, wherein the first portion of the photoresist layer pattern is located on the gate pad.

41. The method of claim 40, wherein etching the metal layer, the ohmic contact layer and the first insulating layer along with the photoresist layer pattern comprises the substeps of:

etching the metal layer, the ohmic contact layer, the semiconductor layer and the first insulating layer under the first portion of the photoresist layer pattern by using the second and the third portions as an etch stopper;

removing the second portion of the photoresist layer to expose the metal layer thereunder by ashing process; and

etching the exposed portion of the metal layer, and the ohmic contact layer and the semiconductor layer thereunder by using the third portion of the photoresist layer as an etch stopper.

42. The method of claim 33, wherein the semiconductor layer is made of amorphous silicon.

43. The method of claim 33, wherein the second insulating layer is made of a photo-definable material.

44. A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising the steps of:

forming a gate wire including a plurality of gate lines and a plurality of gate pads connected to the gate lines on a substrate having a display area and

a peripheral area, the gate lines located substantially in the display area and the gate pads located substantially in the peripheral area;

depositing sequentially a gate insulating layer, a semiconductor layer, an ohmic contact layer and a conductor layer on the gate wire;

coating a photoresist layer on the metal layer;

forming a photoresist layer pattern of which thickness varies depending on the location by exposure and development;

patterning the metal layer, the ohmic contact layer, the semiconductor layer and the gate insulating layer at a time to form a metal layer pattern, a first ohmic contact layer pattern and a semiconductor layer pattern exposing the gate pads by a photolithography process;

depositing a conductor layer;

forming a conductor layer pattern including a plurality of pixel electrodes covering parts of the metal layer and a plurality of separated conductor layer patterns covering the other part of the metal layer and located at the opposite side of the pixel electrodes with respect to the gate electrodes by a photolithography process;

removing the portions of the metal layer between the pixel electrodes and the separated conductor layer patterns and the ohmic contact layer thereunder to form a data wire including a plurality of data lines, data pads, source electrodes and drain electrodes, and a second ohmic contact layer pattern thereunder; and

forming a passivation layer.

45. The method of claim 44, wherein the photoresist layer pattern is

formed only in the display area or on the metal layer pattern, the photoresist layer pattern is thicker on the metal layer pattern than elsewhere of the display area, and patterning the metal layer, the ohmic contact layer, the semiconductor layer and the gate insulating layer at a time comprises the substeps of:

removing the exposed portion of the metal layer in the peripheral area to expose the ohmic contact layer;

removing the thin photoresist layer in the display area to expose the metal layer thereunder using an etch method that can etch the photoresist layer, the ohmic contact layer and the semiconductor layer at a time;

removing the exposed portion of the metal layer in the display area to expose the ohmic contact layer; and

etching the ohmic contact layer, the semiconductor layer and the gate insulating layer to expose the gate pad in the peripheral area and to remove the exposed portion of the ohmic contact layer and the semiconductor layer thereunder using an etch method that is able to etch the ohmic contact layer, the semiconductor layer and the gate insulating layer at a time.

46. The method of claim 44, wherein the passivation layer has openings exposing the pixel electrode.

47. The method of claim 46, wherein the conductor layer pattern includes a plurality of redundant data lines covering the data line, redundant data pad covering the data pad and redundant gate pad covering the gate pad.

48. The method of claim 47, wherein the passivation layer has openings exposing the redundant gate pad and the redundant data pad.

49. The method of claim 44, further including forming on the substrate

a common wire including a plurality of common electrodes generating electric fields with the pixel electrode.

50. A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising the steps of:

forming a gate wire including a plurality of gate lines, gate electrodes connected to the gate line and a common wire including a plurality of common electrodes on an insulating substrate;

forming a gate insulating layer pattern that covers the gate wire and the common wire;

forming a semiconductor pattern on the gate insulating layer;

forming an ohmic contact layer pattern on the semiconductor pattern;

forming a data wire including a plurality of data lines, source electrodes connected to the data line, drain electrodes separate from the source electrode on the ohmic contact layer pattern;

forming a passivation layer pattern covering the data wire except for a part of the drain electrode; and

forming a plurality of pixel electrodes connected to the drain electrodes and generating electric fields with the common electrode,

wherein the source electrode and the drain electrode are separated by a photolithography process of using a photoresist layer pattern, which includes a first portion located between the source electrode and the drain electrode, a second portion thicker than the first portion and a third portion thinner than the first portion.

51. The method of claim 50, wherein the data wire, the ohmic contact

layer and the semiconductor layer are formed using a mask.

52. The method of claim 51, wherein forming the gate insulating layer, the semiconductor pattern, the ohmic contact layer pattern and the data wire further comprises the substeps of:

depositing the gate insulating layer, the semiconductor layer, the ohmic contact layer and the metal layer;

coating a photoresist layer on the metal layer;

exposing the photoresist layer through the photomask;

developing the photoresist layer to form the photoresist layer pattern of which the second portion is located on the data wire;

etching the portion of the metal layer, the ohmic contact layer and the semiconductor layer under the third portion, the second portion along with the portion of the metal layer and the ohmic contact layer thereunder, and some thickness of the second portion to form the data wire, the ohmic contact layer pattern and the semiconductor pattern; and

removing the photoresist layer pattern.

53. The method of claim 52, wherein forming the data wire, the ohmic contact layer pattern and the semiconductor pattern further comprises the substeps of:

etching the portion of the metal layer under the third portion to expose the ohmic contact layer by wet etch or dry etch;

dry etching the ohmic contact layer under the third portion and the semiconductor layer thereunder along with the first portion to expose the gate insulating layer under the third portion and the metal layer under the first portion

along with completing the semiconductor pattern; and

etching the portion of the metal layer under the first portion and the ohmic contact layer thereunder to complete the data wire and the ohmic contact layer pattern.